SPIRIT

SPIKING NEURAL NETWORKS ENABLING MASSIVELY PARALLEL, LOW-POWER & LOW-LATENCY COMPUTATION

WHAT IS SPIRIT?

CEA-Leti introduces SPIRIT, the world-first fully integrated neural network on-chip with non-volatile resistive memory. So far, memories were placed outside of chips leading to high energy consumption. With this co- integration in the same die of analog spiking neurons and resistive synapses leveraging resistive random access memory cells (RRAM), CEA-Leti enables the push for distributed computing devices to support artificial intelligence at the edge.

These spiking neural networks are designed by CEA-Leti and the RRAM are fabricated in a post-process at CEA-Leti on CMOS-based wafers.
SPIRIT is programmed using CEA-List tool N2D2.*

** N2D2 is a open source CAD framework for Deep Neural Network simulation and full DNN-based applications building.*

APPLICATIONS

SPIRIT allows massively parallel, low-power and low-latency computation. It is a perfect candidate for embedded classification applications required in Lidars or IoT devices. The technology also finds applications in event-based sensors packed with rich temporal content.

WHAT'S NEW?

Spiking neural networks are considered as the third generation of neural networks. SPIRIT enables non-volatile, high density and computational memories on the chip. This has been made possible thanks to the Back-End-Of-Line (BEOL), CMOS compatible, resistive memories developed and fabricated at CEA-Leti.
The demonstration features a neural network—perceptron—trained offline for handwritten digits classification. The circuit operates live classification of digits drawn on a touch screen. Spike coding reduces activity translating into less power dissipation, with less than one spike generated per synaptic connection.

WHAT'S NEXT?

In collaboration with CEA-List, CEA-Leti keeps working on improving the resistive RAM technology, especially the integration density. Work is ongoing on the development of a BEOL selector to enable mega-bit scale crossbars, which are the ultimate structure density-wise. CEA-Leti is also pursuing the implementation of mutiple-level cells, i.e. several bits per cell.

This demonstration represents the first milestone of CEA-Leti's roadmap for large spiking neural network accelerators leveraging resistive memories. The next step will consist in interfacing accelerators with event-based vision sensors and LIDARs to enable pose estimation, simultaneous localization and mapping (SLAM), and object classification.

A prototype will be available in 2021.

KEY FACTS

- 3.6pJ per synaptic event (at neuron-level)
- High RRAM synapse robustness to spiking events (1 billion spikes reached without any impact)
- 3 patents pending

INTERESTED IN THIS TECHNOLOGY?

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